Divide-By-Two CMOS/TTL Test-Circuit Description:

This circuit is not guaranteed to meet any specifications, and serves only as an example of a module I built for my own pleasure and enjoyment. It is designed to connect to the LTE-Lite Evaluation board.

Some comments:

* I grab the 3.0V for the 74LVX74 power from capacitor C6 on the LTE-Lite eval board. Please refer to the schematics of the LTE-Lite evaluation board. That capacitor is the low-noise filtered analog supply. By loading it with the FF, that voltage goes down to 2.86V. Using the digital 3.3V supply resulted in excessive spurs so that was abandoned.

* I used only two additional components: a cap and a series resistor. Use a 10nF cap in parallel to a 1uF to 4.7uF SMT cap for low AM noise.

* The IC I used was an old Fairchild 74LVX74 SO-14 chip I had laying around

* Notice the nice improvement in phase noise, and the absence of any measurable spurs

* Notice the nice 6dB phase noise improvement compared to using the direct outptut, even the floor improved to close to my reference noise floor, so theory meets practice

* I spent less than 45 minutes building this on a small copper-clad board, using the ground of the board as much as possible
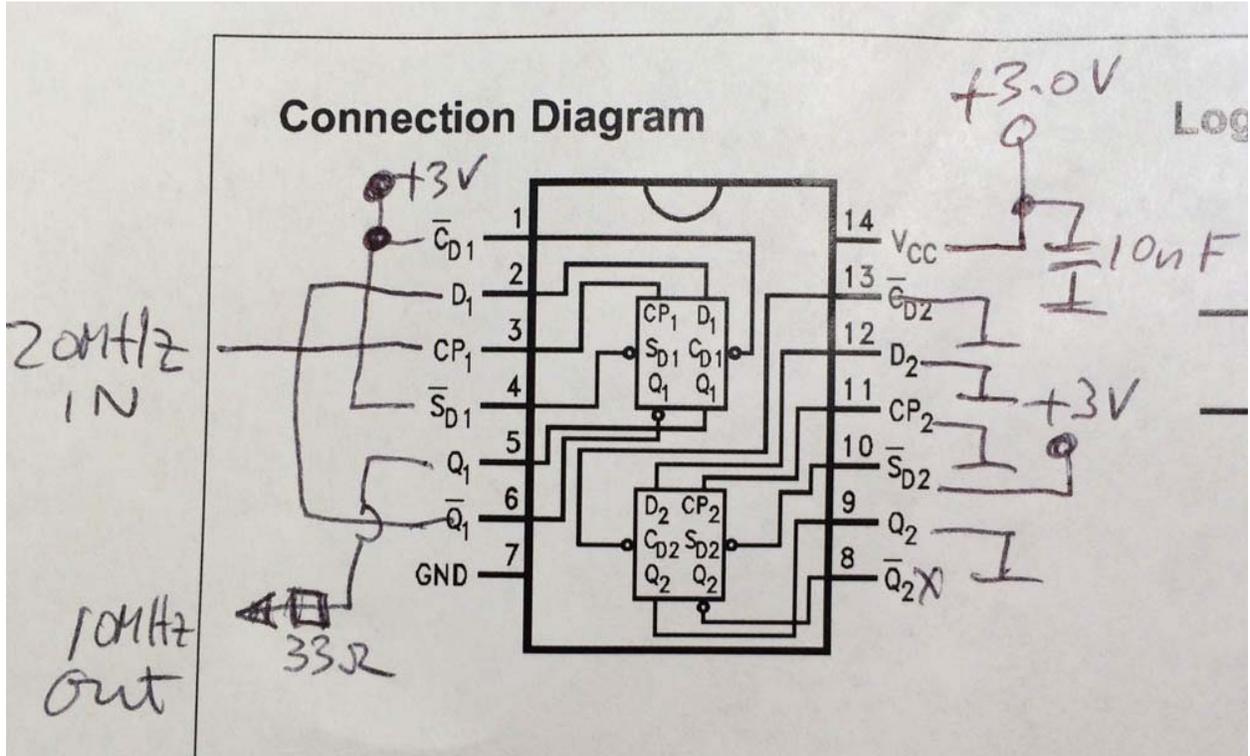
* The output power of the 74LVC74 driving the 50 Ohms input impedance of the analyzer is pretty low, less than 7dBm, so a nice buffer would help. Make sure to use a DC-block before going into spectrum analyzers or phase noise analyzers to avoid analyzer damage.

* Notice how I set the Q output of the unused FF to 0V, and then connect that pin to ground to use it as an additional ground pin
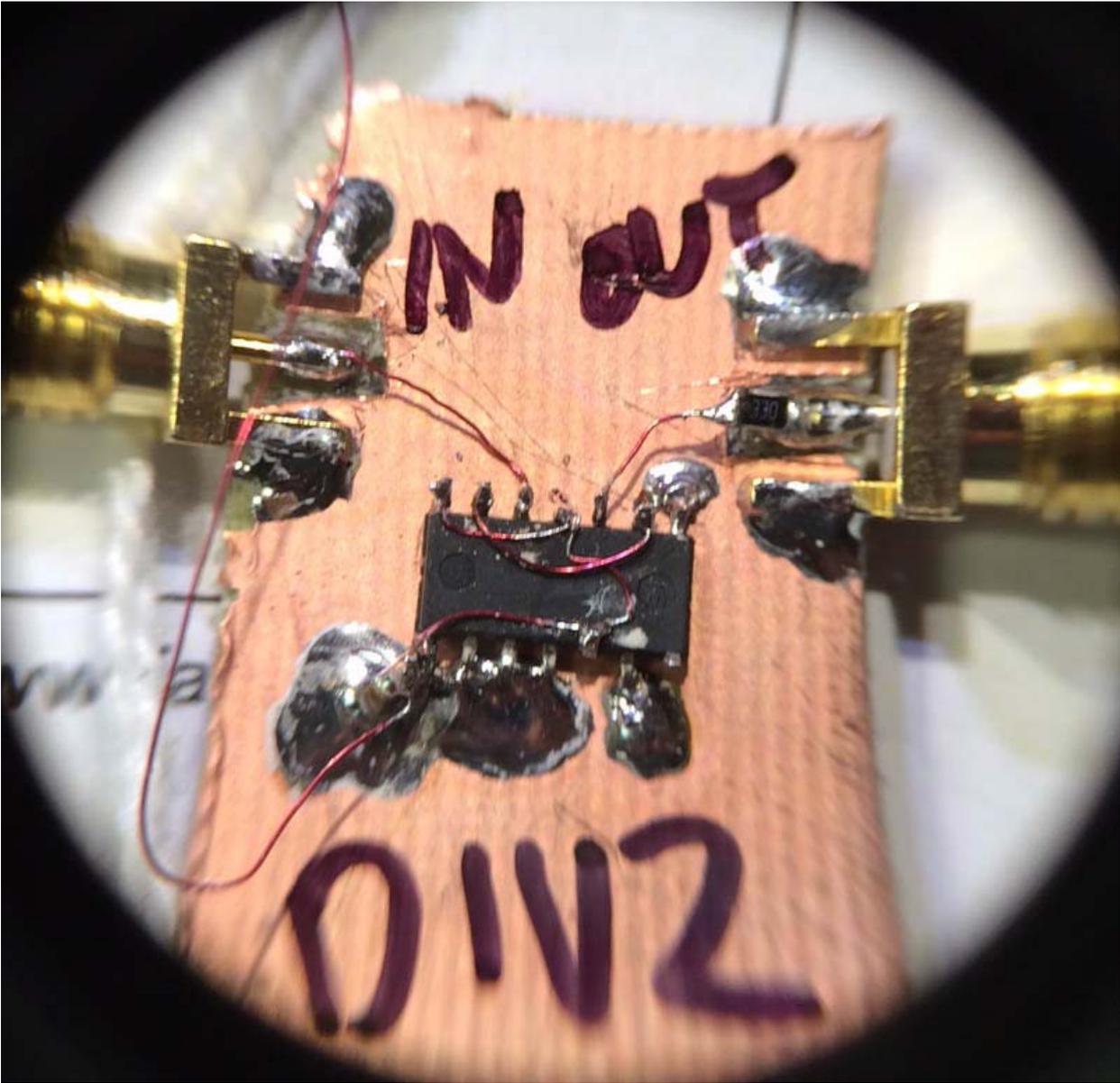
* While I wired up the 3.0V power to the eval board, I did not even bother wiring up the ground. I simply used the coax cables as DC ground return

* The LTE-Lite board was powered from a Thinkpad PC via USB cable, and disciplining to GPS so I did not even use an external low-noise isolated 5V lab supply or anything like that, just the noise PC's USB port.

Schematics of example circuit:

Connection Diagram

+3V

Pin	Label		Pin	Label
1	$\overline{C}_{D1}$		14	V_{CC}
2	D_1		13	$\overline{C}_{D2}$
3	CP_1		12	D_2
4	$\overline{S}_{D1}$		11	CP_2
5	Q_1		10	$\overline{S}_{D2}$
6	$\overline{Q}_1$		9	Q_2
7	GND		8	$\overline{Q}_2$

CP_1 D_1
S_{D1} C_{D1}
Q_1 Q_1

D_2 CP_2
C_{D2} S_{D2}
Q_2 Q_2

+3.0V

Log

10nF

+3V

20MHz IN

10MHz Out

33Ω

Example prototype:

Example setup:
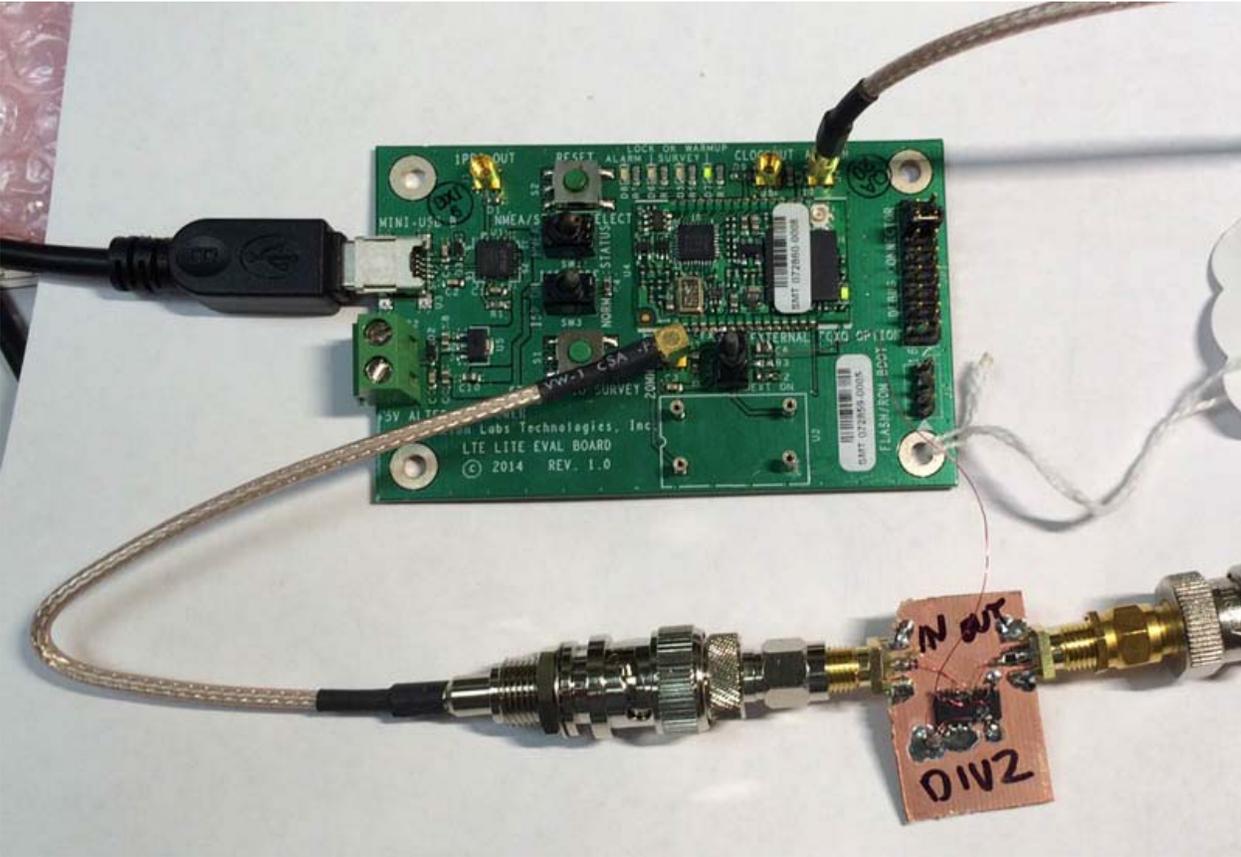
Example Phase Noise at 20MHz and 10MHz:

Phase Noise L(f) in dBc/Hz

Trace	Input Freq	Input Amplitude	Ref Freq	Ref Amplitude	Sample Interval	dBc/Hz at 100 Hz	RMS Jitter	Duration	Acquired	Instrument
(Unsaved)	10.000 MHz	6.6 dBm	10.000 MHz	14.5 dBm	0.100 s	−124.1	2.0E−13 s	38m 7s	22867 pts	TimePod 5330A
(Unsaved)	20.000 MHz	9.9 dBm	10.000 MHz	14.5 dBm	0.100 s		1.6E−13 s	31m 3s	186530 pts	TimePod 5330A
(Unsaved)	20.000 MHz	9.9 dBm	10.000 MHz	14.5 dBm	0.100 s	−117.9	1.6E−13 s	6m 59s	4186 pts	TimePod 5330A